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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/655,423	09/04/2003	Mu-Kyoung Jung	SAM-0428	6706

7590 08/15/2005

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EXAMINER	
TRAN, BINH X	
ART UNIT	**PAPER NUMBER**
1765	

DATE MAILED: 08/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/655,423	JUNG ET AL.	
	Examiner	Art Unit	
	Binh X. Tran	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/7/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Parikh (US 6,225,207).

Respect to claims 1 and 5, Hu discloses a method for manufacturing a semiconductor device having capacitance component region and resistance component region, comprising:

forming a mask layer (320) on an insulating layer (318, 316, 314 or 312) formed on a semiconductor substrate (310);

forming a first photoresist layer pattern (322) on the mask layer, so that a portion of the mask layer formed in the first region and a portion of the mask layer formed in the second region are exposed (Fig 3-A);

performing a first etching process using the first photoresist layer (322) pattern as an etching mask, so that a mask layer pattern, in which the first region and a second

region are exposed, is formed, and a first trench (324) and a second trench (326) having the first thickness are formed in the first region and the second region respectively (Fig 3B, col. 7 line 13-28);

removing the first photoresist layer pattern (322) (See Fig 3C, col. 7 lines 28-30);

forming a second photoresist layer pattern (330), which the first trench (325) of the first region is covered and in which the second trench (326) and portions of the mask layer pattern (320) are exposed (Fig 3D, col. 7 lines 31-49);

performing a second etching process using the second photoresist pattern (330) and the mask layer pattern (320) as an etching mask, so that a third trench (332) having a second thickness thicker that the first thickness is formed in the second region (Fig 3E, col. 7 lines 50-63);

removing the second photoresist pattern (330) (col. 7 lines 64-65);

filling the first and the third trench with metal layer (Fig 3F, col. 7 lines 65-67);

removing portions of the metal layer (350), so that the first metal interconnection and a second metal interconnection are formed inside of the first trench and the third trench respectively (Fig 3G).

Respect to claims 2 and 6, Parikh discloses the metal is copper (col. 16 lines 64-66). Respect to claim 3 and 7, Parikh discloses the copper layer is formed using an electroplating method (col. 16 line 65 to col. 17 line12). Respect to claims 4 and 8, Parikh teaches to use chemical mechanical polishing (CMP) to remove the metal layer (350) (col. 8 lines 1-3).

3. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Hu (US 2003/0001266 A1).

Respect to claim 1, Hu discloses a method for manufacturing a semiconductor device having capacitance component region and resistance component region (paragraph 0003), comprising:

performing a first etching process to an insulating layer (110) formed on a semiconductor substrate (105), so that the first and second trenches (112) having the first thickness are formed in the first region and the second region respectively (paragraph 0024, Fig 1A);

performing a second etching process (i.e. two etch steps) process to the second trench, so that a third trench (114) having a second thickness thicker than the first thickness is formed in the second region (paragraph 0025, Fig 1A);

filling the first trench (112) and the third trench (114) with a metal layer (130) (Fig 1E);

removing portions of the metal layer, so that the first metal interconnection and a second metal interconnection are formed inside of the first trench (112) and the third trench (114) respectively (Fig 1F).

Respect to claims 2-3, Hu discloses the metal layer (130) is copper using electroplating method (paragraph 0039-0040). Respect to claim 4, Hu teaches to use chemical mechanical polishing (CMP) to remove a portion of the metal layer (130) (See paragraph 0041).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh X. Tran whose telephone number is (571) 272-1469. The examiner can normally be reached on Monday-Thursday and every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Binh Tran

Binh X. Tran